We Claim:

1. A magnetically differential input circuit to couple a single-ended signal source to a single-ended receiving circuit, the input circuit comprising:

a first terminal to couple to an output of the single-ended signal source;

a second terminal to couple to a signal return;

a third terminal to couple to an output of the single-ended signal source;

a first loop comprising the first terminal and the second terminal; and

a second loop comprising the second terminal and the third terminal.

2. The magnetically differential input circuit defined in Claim 1, wherein the first loop and the second loop circumscribe substantially equal areas and are arranged so that a first interfering signal induced in the first loop by a source of interference is cancelled by a second interfering signal induced in the second loop by the source of interference.

3. A magnetically differential input circuit as defined in Claim 2, further comprising:

an input node to couple to the receiving circuit;

a common node;

a first conductor coupling the first terminal to the input node;

a second conductor coupling the third terminal to the input node; and

a third conductor coupling the third terminal to the first terminal..

4. A magnetically differential input circuit as defined in Claim 3, wherein:

the first loop comprises:

the first terminal;

the input node;
the first conductor;
the second terminal; and
a first segment of the third conductor; and wherein:
the second loop comprises:
the second terminal;
the input node;
the second conductor;
the third terminal; and
a second segment of the third conductor.

5. A magnetically differential input circuit as defined in Claim 3, further comprising:
a terminating impedance coupled between the input node and the second terminal.

6. A magnetically differential input circuit as defined in Claim 5, wherein the first loop comprises:
the first terminal;
the first conductor;
the input node;
the terminating impedance;
the second terminal; and
a first segment of the third conductor; and wherein:
the second loop comprises:
the second terminal;
the terminating impedance;

the input node;

the second conductor;

the second terminal; and

a second segment of the third conductor.

7. A magnetically differential input circuit as defined in Claim 1, wherein the terminals are substantially collinearly juxtaposed and the second terminals is disposed intermediate between, and substantially equidistant from, the first terminal and the third terminal

8. The magnetically differential input circuit defined in Claim 7, wherein the first loop and the second loop circumscribe substantially equal areas and are arranged so that a first interfering signal induced in the first loop by a source of interference is cancelled by a second interfering signal induced in the second loop by the source of interference.

9. A magnetically differential input circuit as defined in Claim 8, further comprising:

a terminating impedance coupled between an input node and the second terminal.

10. A magnetically differential input circuit to couple a source of differential signals to a differential receiving circuit, the input circuit comprising:

a first terminal to couple to a first output of the source of differential signals;

a second terminal to couple to a second output of the source of differential signals;

a third terminal to couple to the first output of the source of differential signals;

an input node;

a return node;

a first conductor coupled to the first terminal and the input node;

a second conductor coupled to the first terminal and the input node, wherein the terminals, circuit nodes and conductors are arranged to form a first loop and a second loop that effect cancellation of an induced interfering voltage at the receiving circuit.

11. A magnetically differential input circuit as defined in Claim 10, the first loop circumscribes a first area that is substantially equal to a second area circumscribed by the second loop.

12. A magnetically differential input circuit as defined in Claim 11, wherein the first loop comprises:

the first terminal;

the first conductor;

the input node;

the return node;

the second terminal; and

a first segment of the third conductor.

13. A magnetically differential input circuit as defined in Claim 11, wherein the second loop comprises:

the second terminal;

the return node;

the input node;

the second conductor;

the third terminal; and

a second segment of the third conductor.

14. A magnetically differential input circuit as defined in Claim 13, wherein the first loop comprises:

the first terminal;

the first conductor;

the input node;

the return node;

the second terminal; and

a first segment of the third conductor.

15. A magnetically differential input circuit as defined in Claim 10, wherein the first loop comprises:

the first terminal;

the first conductor;

the input node;

the return node;

the second terminal; and

a first segment of the third conductor.

16. A magnetically differential input circuit as defined in Claim 15, wherein the second loop comprises:

the second terminal;

the return node;

the input node;

the second conductor;

the third terminal; and

a second segment of the third conductor.

17. A magnetically differential input circuit as defined in Claim 16, wherein the first loop comprises:

the first terminal;

the first conductor;

the input node;

the return node;

the second terminal; and

a first segment of the third conductor.

18. A magnetically differential input circuit as defined in Claim 11, further comprising:

a first terminating resistance coupled between the input node and the return node; and

a second terminating resistance coupled between the return node and the second terminal.

19. A magnetically differential input circuit as defined in Claim 18, where:
the first loop comprises the first terminating resistance and the second terminating resistance; and
second loop comprise the first terminator resistance and the second.

20. A magnetically differential input circuit as defined in Claim 19, wherein the first loop comprises:
the first terminal;
the first conductor;
the input node;
the return node;
the second terminal; and
a first segment of the third conductor.

21. A magnetically differential input circuit as defined in Claim 19, wherein the second loop comprises:
the second terminal;
the return node;
the input node;
the second conductor;
the third terminal; and
a second segment of the third conductor.

22. A magnetically differential input circuit as defined in Claim 21, wherein the first loop comprises:

the first terminal;

the first conductor;

the input node;

the return node;

the second terminal; and

a first segment of the third conductor.

23. A magnetically and electrically differential input circuit to couple to a differential signal source, the input circuit comprising:

a first input node to couple to a first polarity signal from the signal source;

a second input node to couple to a second polarity signal from the signal source;

a first terminal coupled to the first input node;

a second terminal coupled to the second input node;

a third terminal coupled to the first input node; and

a fourth terminal coupled to the second input node, wherein the first terminal and the fourth terminal are included in a first loop and wherein the second terminal and the third terminal are included in a second loop that opposes to the first loop.

24. An input circuit as defined in Claim 23, further comprising:

coupling means in proximity to the first, second, third and fourth terminals for balancing coupling to the first, second, third and fourth terminals.

25. An input circuit as defined in Claim 24, wherein the coupling means comprises a fifth terminal and a conductor disposed between the second terminal and the fourth terminal.

26. An input circuit as defined in Claim 25, wherein the fifth terminal is coupled to GND.

27. An input circuit as defined in Claim 25, wherein the coupling means comprises a sixth terminal and a conductor disposed in proximity to the first terminal.

28. An input circuit as defined in Claim 27, wherein the sixth terminal is coupled to GND.

29. An input circuit as defined in Claim 28, wherein the coupling means comprises a seventh terminal and a conductor disposed in proximity to the third terminal.

30. An input circuit as defined in Claim 29, wherein the seventh terminal is coupled to GND.

31. An input circuit as defined in Claim 24, further comprising:

first terminating impedance coupled between the first terminal and the fourth terminal; and

second terminating impedance coupled between the second terminal and the third terminal.

32. An input circuit as defined in Claim 31, further comprising a conductor coupled between the first terminal and the third terminal.

33. An input circuit as defined in Claim 32, wherein the first terminating impedance comprises:

a first resistance coupled between the first terminal and GND; and

a second resistance coupled between GND and the fourth terminal.

34. An input circuit as defined in Claim 33, wherein the second terminating impedance comprises:

a third resistance coupled between the second terminal and GND; and

a fourth resistance coupled between GND and the third terminal

35. An integrated receiver comprising:

an amplifier; and

a magnetically differential input circuit coupled to an amplifier input, the input circuit to couple the amplifier to a source of signals and comprising:

a first loop traversing the amplifier input; and

a second loop traversing the amplifier input in a manner that opposes the first loop.

36. The integrated receiver defined in Claim 35, wherein the second loop opposes the first loop in a manner that causes cancellation of an interfering signal.

37. The integrated receiver defined in Claim 35, wherein the input circuit comprises:

a first terminal to couple to an output of a single-ended signal source;

a second terminal to couple to a signal return;

a third terminal to couple to the output of the single-ended signal source, wherein the first loop includes the first terminal and the second terminal and the second loop includes the second terminal and the third terminal.

38. The integrated receiver defined in Claim 37, wherein the first loop and the second loop circumscribe substantially equal areas and are arranged so that a first interfering signal induced in the first loop by a source of interference is cancelled by a second interfering signal induced in the second loop by the source of interference.

39. The integrated receiver defined in Claim 35, wherein the input circuit comprises:

a first terminal to couple to a first output of a source of differential signals;

a second terminal to couple to a second output of the source of differential signals;

a third terminal to couple to the first output of the source of differential signals;

an input node;

a return node;

a first conductor coupled to the first terminal and to the input node; and

a second conductor coupled to the first terminal and to the input node, wherein the terminals, circuit nodes and conductors are arranged to form a first loop and a second loop that effect cancellation of an induced interfering voltage at the amplifier input.

40. A The integrated receiver defined in Claim 39, wherein the first loop circumscribes a first area that is substantially equal to a second area circumscribed by the second loop.

41. A magnetically differential input circuit as defined in Claim 40, wherein the first loop comprises:

the first terminal;

the first conductor;

the input node;

the return node;

the second terminal; and

a first segment of the third conductor.

42. The integrated receiver defined in Claim 40, wherein the second loop comprises:

the second terminal;

the return node;

the input node;

the second conductor;

the third terminal; and

a second segment of the third conductor.

43. The integrated receiver defined in Claim 35, further comprising coupling means for causing the input circuit to effect electrically differential operation.

44. The integrated receiver defined in Claim 43, wherein the input circuit comprises:

a first input node to couple to a first polarity signal from the source of signals;

a second input node to couple to a second polarity signal from the source of signals;

a first terminal coupled to the first input node;

a second terminal coupled to the second input node;

a third terminal coupled to the first input node; and

a fourth terminal coupled to the second input node, wherein the first terminal and the fourth terminal are included in the first loop and wherein the second terminal and the third terminal are included in the second loop.

45. The integrated receiver defined in Claim 44, wherein the coupling means is disposed in proximity to the first, second, third and fourth terminals to balance coupling to the first, second, third and fourth terminals.

46. The integrated receiver defined in Claim 45, wherein the coupling means comprises a fifth terminal and a conductor disposed between the second terminal and the fourth terminal.

47. The integrated receiver defined in Claim 46, wherein the coupling means comprises a sixth terminal and a conductor disposed in proximity to the first terminal.

48. The integrated receiver defined in Claim 47, wherein the coupling means comprises a seventh terminal and a conductor disposed in proximity to the third terminal.